

The diagram illustrates a system architecture. On the left, a box labeled "MACHINE" (10) contains "REGISTERS" (12) and "FLAGS" (14). A central vertical bus (16) is labeled "1/2" at the top. To the right of the bus, there are four components: "READ-ONLY MEMORY" (18) containing an "ERROR HANDLER" (20), "RANDOM ACCESS MEMORY" (22), and two "PERIPHERAL DEVICE" (24) blocks. Bidirectional arrows indicate communication between the machine and the bus, and between the bus and each of the four components on the right.

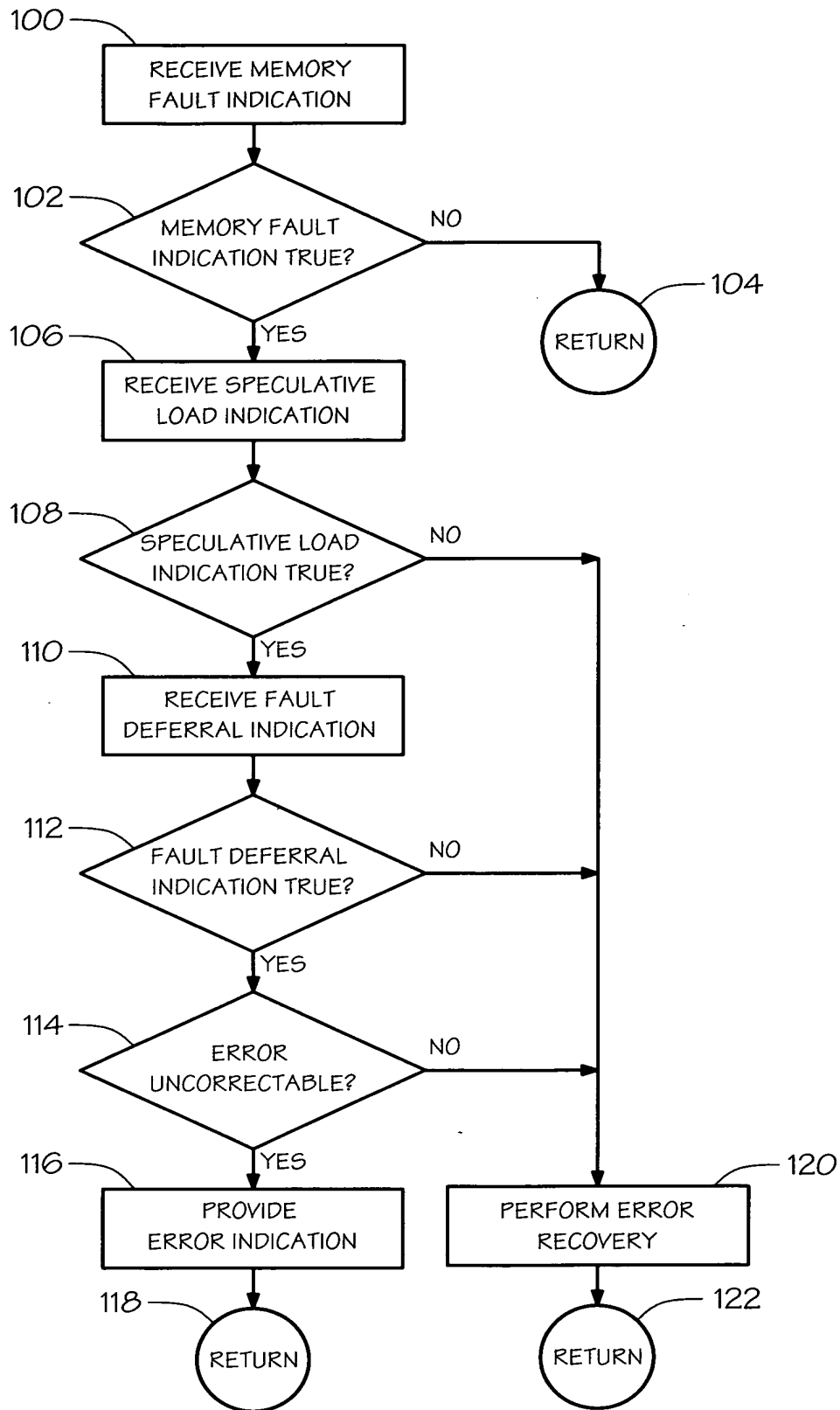


FIG. 2